REMARKS

Claims 1 to 25 were pending in the present application when last examined. Applicant has amended claims 2 to 7 and 12 to 25, canceled claims 1 and 8 to 11, and added claim 26. Claims 2 to 7 and 12 to 26 are now pending.

§ 103 Rejections

The Examiner rejected claims 1 to 25 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in view of U.S. Patent No. 6,833,728 ("Chennupati").

Claims 1 and 2

Addressing claim 1, the Examiner stated:

> … AAPA teaches an integrated circuit comprising:
>
> A plurality of pins (Drawings, Fig. 1, ref. 2, 12); and
>
> A scan path (Drawings, Fig. 1, ref. 9) coupled to the pin (input pin 2 of Fig. 1)
>
> AAPA does not teach the integrated circuit comprising at least one respective scan path per pin.
>
> Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25), therefore the bi-directional pin have a data path for receiving data and another data path for output data (Fig. 1, ref. 156).
>
> It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's each respective plurality of pins. The resulting combination of the references teaches the integrated circuit further comprising each pin having the scan path for receiving data and another scan path for outputting data.

12/6/06 Final Office Action, p. 4. Addressing claim 2, the Examiner stated:

> … AAPA and Chennupati teach all the limitation of claim 1 as discussed above, where both further teach the integrated circuit comprising wherein:
>
> a first I/O pin is operable to input scan test data at a first test time (AAPA, Specification, p. 1, ll. 5-6 and Chennupati, Fig. 1, ref. 152; col. 1, ll. 15-17 and col. 4, ll. 23-25); and
>
> the first I/O pin is operable to output scan test data at a second test time (AAPA, Specification, page 1, ll. 5-6 and Chennupati, Fig. 1, ref. 152;

col. 1, ll. 15-17 and col. 4, ll. 23-25), as the receiving and the outputting of the test data is transferred through the same I/O pin.

12/6/06 Final Office Action, p. 5.

Applicant has canceled claim 1 and amended claim 2 to include the limitations of claim 1 and to further clarify the claimed invention. Accordingly, Applicant addresses the rejections of claims 1 and 2 together. Amended claim 2 now recites:

> 2. An integrated circuit, comprising:
>
> a scan path having an input and an output; and
>
> a pin coupled to the input and the output of the scan path, wherein:
>
> the I/O pin inputs scan test data to the scan path at a first test time; and
>
> the I/O pin outputs scan test data from the scan path at a second test time.

Amended claim 2 (emphasis added). One embodiment of amended claim 2 is shown in Figs. 5 and 6C where a pin 31 is coupled to input and output of a scan path 36.

Assuming that Chennupati is analogous art, the combination of the AAPA and Chennupati still does not disclose the integrated circuit as recited in amended claim 2. The Examiner argued that one skilled in the art would replace input pad 2 and output pad 12 of scan path 9 in Fig. 1 of the AAPA with bidirectional pins of Chennupati. Such a modification results in a scan path 9 coupled between bidirectional pads 2 and 12. However, amended claim 2 now recites a pin that is coupled to both the input and the output of the same scan path to provide input scan test data to the scan path at a first test time and to provide output scan test data from the scan path at a second test time. Accordingly, amended claim 2 is patentable over the combination of the AAPA and Chennupati.

Claims 3 and 4

Addressing claim 3, the Examiner stated:

> … AAPA and Chennupati teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit comprising:
>
> the first I/O pin (I/O pin couple to L0 of Fig. 2) is operable to input scan test data to a first scan path at the first test time (Chennupati, col. 5, ll. 38-44), wherein the WRITE0 data is received through L0 bus line;

a second I/O pin (I/O pin coupled to L1 of Fig. 2) is operable to input scan test data to a second scan path at the first test time (Chennupati, col. 5, ll. 38-44), wherein the WRITE1 data is received through the L1 bus line;

the first I/O pin (I/O pin couple to L0 of Fig. 2) is operable to output scan test data from the second scan path at the second test time (Chennupati, col. 5, ll. 38-44), wherein the READ1 data is to be outputted to the L0 bus line;

the second I/O pin (I/O pin coupled to L1 of Fig. 2) is operable to output scan test data from the first scan path at the second test time (Chennupati, col. 5, ll. 38-44), wherein the READ0 is to be outputted to the L1 bus line.

12/6/06 Office Action, pp. 5 and 6.

Applicant has amended claim 3 to include the limitations of claims 1 and 2 and to further clarify the claimed invention. Amended claim 3 now recites:

3. An integrated circuit, comprising:

a first scan path;

a second scan path;

a first I/O pin inputting input scan test data to an input of the first scan path at a first test time and outputting output scan test data from an output of the second scan path at a second test time; and

a second I/O pin inputting input scan test data to an input of the second scan path at the first test time and outputting output scan test data from an output of the first scan path at the second test time.

Amended claim 3. One embodiment of amended claim 3 is shown in Fig. 6a where a first pin 31 is coupled to an input of a first scan path 36 and an output of a second scan path 41, and a second pin 30 is coupled to an input of second scan path 41 and an output of first scan path 36.

As discussed above with regards to claim 2, the Examiner argued that one skilled in the art would replace input pad 2 and output pad 12 of scan path 9 in Fig. 1 of the AAPA with bidirectional pins of Chennupati. Such a modification results in one scan path 9 coupled between bidirectional pads 2 and 12. However, amended claim 3 recites a first pin coupled to an input of a first scan path and an output of a second scan path, and a second pin 30 coupled to an input of the second scan path and an output of the first scan path. Furthermore, Chennupati shows that each pair of the bidirectional pins is coupled to a single line instead of two scan paths. Accordingly, amended claim 3 is patentable over the combination of the AAPA and Chennupati.

Amended claim 4 depends from amended claim 3 and is patentable for at least the same reasons as amended claim 3.

Claims 5 to 7

Claims 5 to 7 depend from amended claim 2 and are patentable for at least the same reasons as amended claim 2.

Claims 8 to 11

To expedite prosecution, Applicant has canceled claims 8 to 11. Applicant reserves the right to prosecute these claims in a continuing application.

Claims 12 to 18

Addressing claim 12, the Examiner stated:

> AAPA does not teach the integrated circuit comprising wherein the I/O pin operable to be used as output at a second time, the I/O pin have a respective scan path operable to produce scan output; and further more, does not expressly teach that the flip-flop is coupled to the I/O pin and to the functional circuit and the scan path.
>
> Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25) and the data is inputted into a device (fig. 1, ref. 150) through a respective INPUT2 data path and outputted from the device through a respective OUTPUT2 data path (Fig. 1, ref. 156), wherein the received INPUT2 data would have been processed by other components in the device to generated the OUTPUT2 data to be outputted (Fig. 1 and col. 4, ll. 27-29).
>
> It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's first and second I/O pins.
>
> The resulting combination of the references teaches the integrated circuit further comprising the I/O pin is operable to input scan data at the first time and to output scan data at the second time, as the I/O pin have the respective scan path operable to produce scan output data (e.g., OUTPUT2 data); and further more, it would have been obvious that the D flip-flop is coupled to the I/O pin to obtain the initial seed value, and coupled to the scan path for inputting the scan input data, and coupled to the functional circuit (e.g. components in the device) as the scan input data would be processed by the components before outputting, therefore, implementing the reseeding and provide a more complex self-generating test (AAPA, Specification, page 3, ll. 1-3).

12/6/06 Final Office Action, pp. 11 to 13 (emphasis added). Applicant respectfully traverses.

As discussed above with regards to claim 2, replacing input pad 2 and output pad 12 of scan path 9 of AAPA in Fig. 1 with bidirectional pins of Chennupati would result in a scan path 9

coupled between bidirectional pads 2 and 12. Such a modification is very different from the claimed invention so the Examiner argued that additional modifications are obvious. For example, the Examiner argued it would be obvious to couple flip-flop 20 of Fig. 4 to one of the bidirectional pads to obtain an initial seed value. However, the AAPA and Chennupati provide no suggestion or motivation to do so. The initial seed value may easily be hardwired or stored in memory. Furthermore, the Examiner agued it would be obvious to connect flip-flop 20 of Fig. 4 to a functional circuit. However, the AAPA and Chennupati again provide no suggestion or motivation to do so. The AAPA describes that the reseeding generates scan input data 23, which is intended for a scan path and not the functional circuit in general.

To expedite prosecution and to further clarify the claimed invention, Applicant has amended claim 12. Amended claim 12 now recites:

> 12. An integrated circuit, comprising:
>
> a functional circuit producing functional output;
>
> an I/O pin that acts as input at a first time and as output at a second time, the I/O pin having a respective scan path that produces scan output;
>
> an I/O circuitry, comprising:
>
> an input buffer coupled to (1) the I/O pin to receive input signal and (2) to the functional circuit to provide the input signal;
>
> a virtual pin output buffer coupled to the I/O pin to provide output signal; and
>
> a virtual pin multiplexer coupled to (1) the function circuit to receive the functional output and (2) the scan path to receive the scan output, the virtual pin multiplexer providing a virtual pin multiplexer output;
>
> a virtual pin flip-flop coupled to (1) the virtual pin multiplexer to receive the virtual pin multiplexer output and (2) the virtual pin output buffer to provide the virtual pin multiplexer output, the virtual pin flip-flop holding the received data for a clock cycle.

Amended claim 12. Amended claim 12 now positively claim many of the limitations. For the reasons discussed above and the amendments presented, claim 12 is patentable over the AAPA and Chennupati.

Claims 13 to 18 depend from amended claim 12 and are patentable over the AAPA and Chennupati for at least the same reasons as amended claim 12.

Claims 19 to 25

Claim 19 is a method claim that substantially parallels apparatus claim 2. Thus, claim 19 is patentable over the AAPA and Chennupati for at least the same reasons as claim 2.

Claims 20 to 25 depend from claim 19 and are patentable for at least the same reasons as claim 19.

Summary

In summary, claims 1 to 25 were pending in the present application. Applicant has amended claims 2 to 7 and 12 to 25, canceled claims 1 and 8 to 11, and added claim 26. For the above reasons, Applicant respectfully requests the Examiner to withdraw the claim rejections and allow claims 2 to 7 and 12 to 26. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

I hereby certify that this correspondence is being transmitted prior to expiration of the set period of time by being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

/David C Hsia/ March 3, 2007
Signature Date

Respectfully submitted,

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